

IN THE CLAIMS

Please accept amended claims 1-5, 10-11, 16, 18, 20 and cancel claim 17 without prejudice as follows:

1. (Currently Amended) A data recovery apparatus for recovering effective data from serial data ~~received via a high-speed serial link~~, the data recovery apparatus comprising:

a clock signal generating circuit that generates at least two groups of clock signals ~~groups~~, comprising first and second groups of clock signals ~~groups~~, wherein each of the first and second clock signal groups comprises at least two different inputted clock signals ~~having different phases from each other~~, the first group of clock signals comprising N phase shifted clock signals of an oversampling rate of N, the second group of signals comprising N phase shifted clock signals of the same oversampling rate and being timewise interstitial to the first group of signals, wherein N is greater than 1; and an oversampler to sample the serial data at the oversampling rate of N using a selected one of the clock signal groups to generate sampling data; and

a data recovery circuit that recovers the effective data from the serial data by analyzing the sampling data to determine whether a transition has occurred in the sampling data during clock sections of the currently selected group of clock signals and selecting a different one of the groups of clock signals to be used by the oversampler based on how many of the clock sections the transition has occurred, oversampling the serial data by using a dynamically selected one of the at least two clock signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data.

2. (Currently Amended) The data recovery apparatus of claim 1, wherein the data recovery circuit further comprises:

a clock signal selecting circuit that selects one of the different at least two groups of clock signals groups in response to a clock selection signal,

~~wherein; the~~an oversampler ~~that~~ latches the serial data in response to the selected ~~one of the at least two group of clock signals groups~~ to output NOSR bits of the sampling data per each bit of the serial data; and

~~wherein the clock and~~ data recovery circuit ~~that~~ selects one of the NOSR bits of the sampling data per each bit of the serial data as effective data; and outputs the clock selection signal in response to logic values of the bits of the sampling data.

3. (Currently Amended) The data recovery apparatus of claim 2, wherein the clock signal generating circuit comprises:

a phase-locked loop that generates ~~the at least~~ first and second groups of NOSR sampling phase shifted clock signals ~~each having different phases~~.

4. (Currently Amended) The data recovery apparatus of claim 2, wherein the clock signal generating circuit comprises:

a phase-locked loop that generates the first group of NOSR phase shifted clock signals; and

a sub-clock signal generating circuit that generates the second group of NOSR phase shifted clock signals.

5. (Currently Amended) The data recovery apparatus of claim 1, wherein the first clock signal group comprises ~~OSR~~ sampling clock signals having ~~OSR~~ different phases, wherein ~~NOSR~~ is at least 3, and the second group of clock signals ~~group~~ comprises NOSR clock signals having multiple phases that are all different from the NOSR phases of the first group of clock signals ~~group~~.

6. (Original) The data recovery apparatus of claim 5, wherein the phase-locked loop generates first, second, and third sampling clock signals such that rising edges of the first, second, and third sampling clock signals are arranged at equal intervals, and the sub-clock signal generating circuit generates fourth, fifth, and sixth sampling clock signals so that rising edges of the forth, fifth, and sixth sampling clock signals are arranged at equal intervals.

7. (Original) The data recovery apparatus of claim 5, wherein the sub-clock signal generating circuit comprises:

a first sub-clock signal generating circuit that generates the fourth sampling clock signal in response to the first and second sampling clock signals;

a second sub-clock signal generating circuit that generates the fifth sampling clock signal in response to the second and third sampling clock signals; and

a third sub-clock signal generating circuit that generates the sixth sampling clock signal in response to the first and third sampling clock signals.

8. (Original) The data recovery apparatus of claim 7, wherein the first, second, and third sub-clock signal generating circuits are interpolators.

9. (Original) The data recovery apparatus of claim 6, wherein the rising edge of the fourth sampling clock signal is located between the rising edge of the first sampling clock signal and the rising edge of the second sampling clock signal; the rising edge of the fifth sampling clock signal is located between the rising edge of the second sampling clock signal and the rising edge of the third sampling clock signal; and the rising edge of the sixth sampling clock signal is located between the rising edge of the third sampling clock signal and the rising edge of the first sampling clock signal.

10. (Currently Amended) The data recovery apparatus of claim 5, wherein the clock signal selecting circuit comprises a plurality of multiplexers that receive the first and second groups of clock signals ~~groups~~ and output one of the first and second groups of clock signals ~~groups in response to the clock selection signal~~.

11. (Currently Amended) A data recovery apparatus for recovering effective data from serial data received via a high-speed serial link. ~~The data recovery apparatus comprising:~~

a clock signal generating circuit that generates at least two clock signal groups, comprising first and second clock signal groups, wherein each of the first and second clock signal groups comprises at least two different inputted clock signals having different phases from each other;

a data recovery circuit that recovers the effective data from the serial data by oversampling the serial data by using a dynamically selected one of the at least two clock signal groups, the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data, wherein the data recovery circuit comprises:

a clock signal selecting circuit that selects one of the at least two clock signal groups in response to a clock selection signal;

an oversampler that latches the serial data in response to the selected one of the at least two clock signal groups to output OSR bits of sampling data per each bit of serial data; and

a clock and data recovery circuit that selects one of the OSR bits of sampling data per each bit of serial data as effective data outputs the clock selection signal in response to logic values of the bits of sampling data,

of claim 2, wherein the clock signal group output from the clock signal selecting circuit comprises OSR sampling clock signals having edges that define OSR clock sections between the OSR sampling clock signals; and wherein the clock and data recovery circuit comprises:

a transition-detecting unit that outputs internal signals indicating whether zero-crossing transitions occur during each of the OSR clock sections;

an adder unit that counts the number of times zero-crossing transitions occurs during each of OSR clock sections, accumulates each of the OSR counts for a predetermined period of time, and compares the OSR accumulated counts with each other, and outputs a count signal;

a data selecting unit that outputs a sampling-data selection signal in response to the count signal; and

a data output unit that outputs one of the plurality of sampling data in response to the data selection signal.

12. (Original) The data recovery apparatus of claim 11, wherein the clock signal selecting circuit comprises a clock signal-selecting unit that outputs the clock selection signal in response to the count signal.

13. (Previously Presented) The data recovery apparatus of claim 11, wherein the count signal indicates the clock section having the highest count of the OSR accumulated values, and the data output unit outputs the sampling data latched by the sampling clock signal farthest from the indicated transition part as the effective data in response to the data selection signal.

14. (Original) The data recovery apparatus of claim 13, wherein the clock signal selecting circuit selects, from the at least two clock signal groups comprising the first and second clock signal groups, one clock signal group having a plurality of sampling clock signals having edges within the eye open region of the serial data.

15. (Original) The data recovery apparatus of claim 12, wherein the clock signal selecting unit monitors the count signal and outputs the clock selection signal such that the clock signal selecting unit deselects the currently selected clock signal group used by

the oversampler when all of the OSR clock sections shall have been transition parts.

16. (Currently Amended) A data recovery method for recovering effective data from serial data, the method being performed by an oversampling data recovery apparatus comprising: a clock signal generating circuit that generates at least two clock signal groups, the at least two clock signal groups comprising first and second clock signal groups, each of the first and second clock signal groups comprising at least two different inputted sampling clock signals, wherein each sampling clock signal has a unique phase; and a data recovery circuit that recovers the effective data from the serial data by sampling the serial data by the sampling clock signals of a dynamically selected one of the at least two sampling clock signal groups, wherein the selection of the selected one of the at least two clock signal groups depends on the number of edges of the clock signals of the selected clock signal group being within an eye open region of the serial data,

wherein the at least two clock signal groups each comprise OSR sampling clock signals between the edges of which there are OSR clock sections, the data recovery method further comprising:

sampling and latching OSR bits of sampling data from each bit of the serial data;
counting the number of times a zero-crossing transition occurs in each of the OSR clock sections and accumulating the count value of each of the OSR clock sections;
comparing the OSR accumulated count values and outputting a count signal indicating the clock section having the greatest value among the accumulated count values; and

outputting the sampling data latched by the sampling clock signal farthest from the clock section indicated by the count signal, as the effective data.

17. (Cancelled)

18. (Currently Amended) The data recovery method of claim 17~~16~~, further comprising:

monitoring the count signal to deselect the currently selected one of the at least two sampling clock signal groups when a zero-crossing transition shall have occurred in each of the OSR clock sections; and then resetting the OSR count values and sampling the next received serial data by the sampling clock signals of the newly selected one of the at least two sampling clock signal groups.

19. (Original) The data recovery method of claim 16, wherein one of the at least two clock signal groups is dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data.

20. (Currently Amended) A data recovery method for recovering effective data from an input stream of serial data ~~having an eye open region and a plurality of zero-crossing transitions~~, the method comprising:

oversampling each bit of the serial data at an oversampling rate of OSR using one of a first and second set of phase-shifted sampling clock signals to generate sampling data;

~~and latching OSR bits of the sampling data for each bit of the serial data according to a selected one of the first and second set of OSR sampling clock signals selected from among a first and second set of OSR sampling clock signals, wherein each set of OSR sampling clock signals comprise at least two different inputted phase shifted clock signals and one of the sets is timewise interstitial to the other having different phases from each other; and wherein the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data; and~~

analyzing the latched OSR bits to determine whether a transition has occurred in the sampling data during clock sections of the selected set of OSR sampling clock signals; and

selecting the other set of OSR sampling clocks signals for subsequent oversampling of each bit of the serial data based on how many of the clocks sections the transition has occurred.